

ABSTRACT OF THE DISCLOSURE

In a memory cell, the cell ratio between an N-channel MOS transistor as a driver transistor and an N-channel MOS transistor as an access transistor is 1. To the first and second storage nodes, capacitors are
5 connected, respectively. A word line driver receives a voltage obtained by boosting a power source voltage from a boosted power source voltage generating circuit and activates a word line with the boosted voltage. A bit line precharge circuit precharges bit lines to the power source potential
10 when the word line is inactivated in accordance with a signal outputted from a BLPC signal generating circuit.